

REMARKS

Claims 1-28 are pending in the instant application. Claims 1-28 are rejected.

No new matter has been added.

103 Rejections

Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are recited in Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1. The Claim 1 embodiment of the present invention is drawn to a controller chip comprising:

...a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and a storage element coupled to the graphics engine, the storage element being accessible by a central processing unit (CPU) through the graphics engine, wherein the engine receives commands from the CPU via the integral interface, manages the storage element via the integral interface and writes the commands into the memory and wherein the graphics engine incorporates the storage element as part of the memory.

Independent Claims 11 and 20 recite limitations similar to those of Claim 1. Claims 2, 3, 6, 9 and 10 depend from Claim 1, Claims 12, 13, 16 and 17 depend from Claim 11, and Claims 21, 25 and 26 depend from Claim 20 and set forth additional limitations of the claimed invention.

Dye does not anticipate or render obvious a controller chip that includes a graphics engine a memory, and a storage element wherein the graphics engine is operative to manage the memory and wherein “the graphics engine comprises an integral interface” as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not anticipate or render obvious a controller chip that includes a graphics engine that “receives commands from the CPU via the integral interface, and manages the storage element via the integral interface” as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). It should be appreciated that in order to anticipate or render obvious the embodiment of the invention that is set forth in Claim 1 the cited references must teach or suggest, either expressly or inherently, in addition to all of the other limitation of Claim 1, a graphics engine that: (1) includes an integral interface; (2) receives commands from a CPU via the integral interface that is a part of the engine; and (3) manages a storage element via the same integral interface. The Applicant respectfully submits that such a system structure and operation is neither shown nor suggested by Dye.

Dye discloses a memory controller that includes embedded data compression and decompression engines and that uses data compression to reduce system bottlenecks. However, the system structure that is disclosed by Dye is distinct from that of the system which is set forth in the Applicant’s claims and cannot support significant aspects of the functionality of the system that is defined in Applicant’s claims. Specifically, Dye does not show a controller graphics engine that includes an integral interface that is actually physically integrated into the graphics engine through which commands from a CPU are received and via which a storage element is managed as is set forth in Claim 1.

It should be noted that those components of the Dye system that are intended to represent engines are clearly delineated as such (e.g., labeled as execution engine 210 and graphics engine 212 in Figure 5 of Dye). Neither the execution engine 210 nor the graphics engine 212 are described in the text or shown in the drawings of the Dye reference to have an interface integrally included therein. This should be contrasted with Applicant's specification that describes as is shown in Applicant's Figure 4 that the recited interface is actually a physically integrated part of the recited graphics engine.

Despite obvious fundamental differences between the location and role of the interface logic 202 disclosed by Dye and the interface that is set forth in Applicant's Claim 1 (as was outlined above), the interface logic 202 disclosed by Dye is equated in the rejection with the recited integral interface of the controller graphics engine that is set forth in Applicant's Claim 1. However, the Applicant respectfully submits that because of the fundamental differences outlined above, an interpretation of Dye as teaching or suggesting the embodiment of Applicant's invention as is set forth in Claim 1 that is permissible under well established principles of patent law is precluded.

Davis does not teach or suggest a modification of Dye that remedies the deficiencies of Dye outlined above. More specifically, Davis et al. does not teach or suggest a controller chip that includes a graphics engine, a memory, and a storage element wherein the graphics engine is operative to manage the memory and wherein "the graphics engine comprises an integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not teach or suggest a controller chip that includes a graphics engine that "receives commands from the CPU via the integral interface, and manages the storage element

via the integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations).

Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division channels of a digital carrier signal. It should be appreciated that the Davis et al. reference is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. As a result, nowhere in the Davis et al. reference is there shown a controller chip engine that receives commands via an integral interface and manages a storage element via the interface where the interface is actually a part of the graphics engine itself as is set forth in Claims 1, 11 and 20. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye and Davis et al. either alone or in combination.

Therefore, Applicant respectfully submits that Claims 1, 11 and 20 are in condition for allowance. Accordingly, Applicant respectfully submits that Dye and Davis et al. either alone or in combination, do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 2, 3, 6, 9 and 10 dependent on Claim 1, Claims 12, 13 16 and 17 dependent on Claim 11, and Claims 21, 25 and 26 dependent on Claim 20. Claims 2, 3, 6, 9, 10, 12, 13, 16, 17, 21, 25 and 26 are allowable as they are dependent on allowable base claims.

Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169) and further in view of an Official Notice. The Applicant has reviewed the cited references and respectfully submits that embodiments of the present invention as are recited in

Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al. and further in view of the Official Notice. It should be appreciated that the Official Notice is concerned with the obviousness of utilizing various FIFO buffer geometries but does not address the deficiencies of either Dye or Davis et al. as outlined above. Consequently, the embodiments of the Applicant's invention as set forth in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye in view of Davis et al. and further in view of the Official Notice as these Claims are dependent on base Claims 1, 11 and 20 whose allowability are discussed above.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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